

The Truth about Differential Pairs in High Speed PCBs

IPC DC - RTP Chapter
- PCB Carolina -
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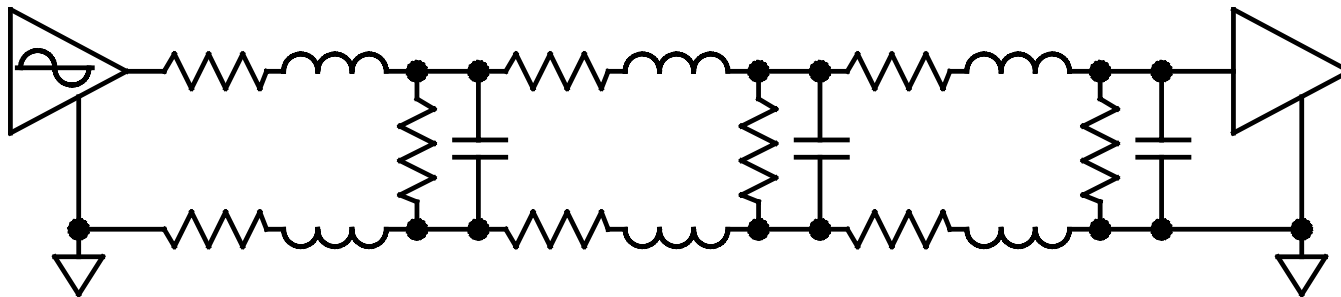
Read Books Not IC App Notes

“Circuit Application notes
produced by IC manufac-
turers should be assumed
Wrong until Proven Right!”

Lee W. Ritchey

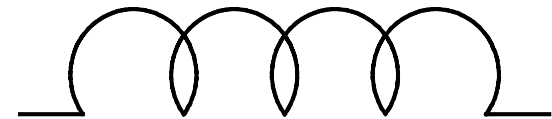
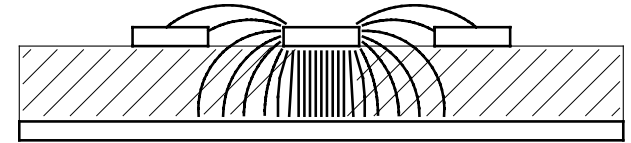
- Transmission Lines -

- A Transmission Line is any Pair or Wires or Conductors used to Move Energy From point A to point B
- Usually of Controlled Size and in a Controlled Dielectric to create a Controlled Impedance (Z_0).



- Transmission Lines -

- Capacitance is formed by 2 conductive surfaces separated by an insulator.
- Control Electric Field in Transmission Line by maintaining tight coupling between the Trace and Return Path.
- Inductance is property of a circuit which allows Energy Storage in a Field Induced by Current Flow.
- Tight coupling between forward and return path are secret to lowering Inductance in Circuit.

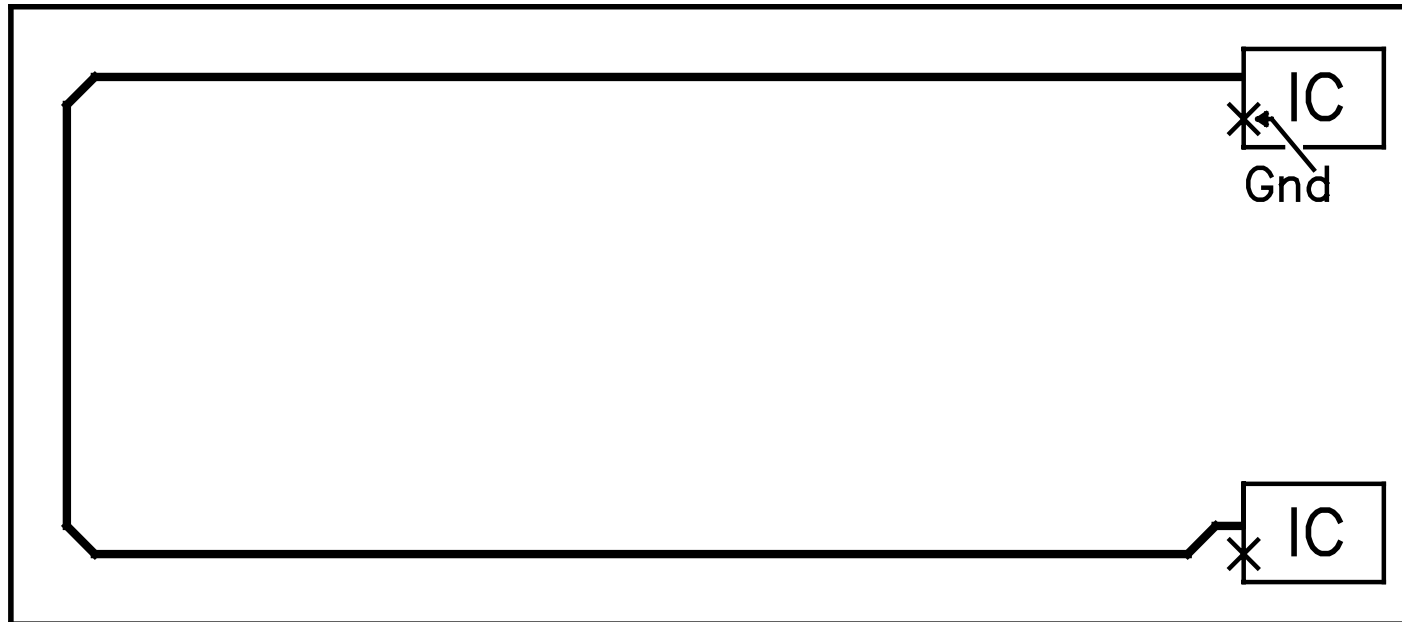


- Transmission Lines -

- 2 Layer Microwave Style PC Board -

L1- Routed Signal, routed Power and poured Ground copper.

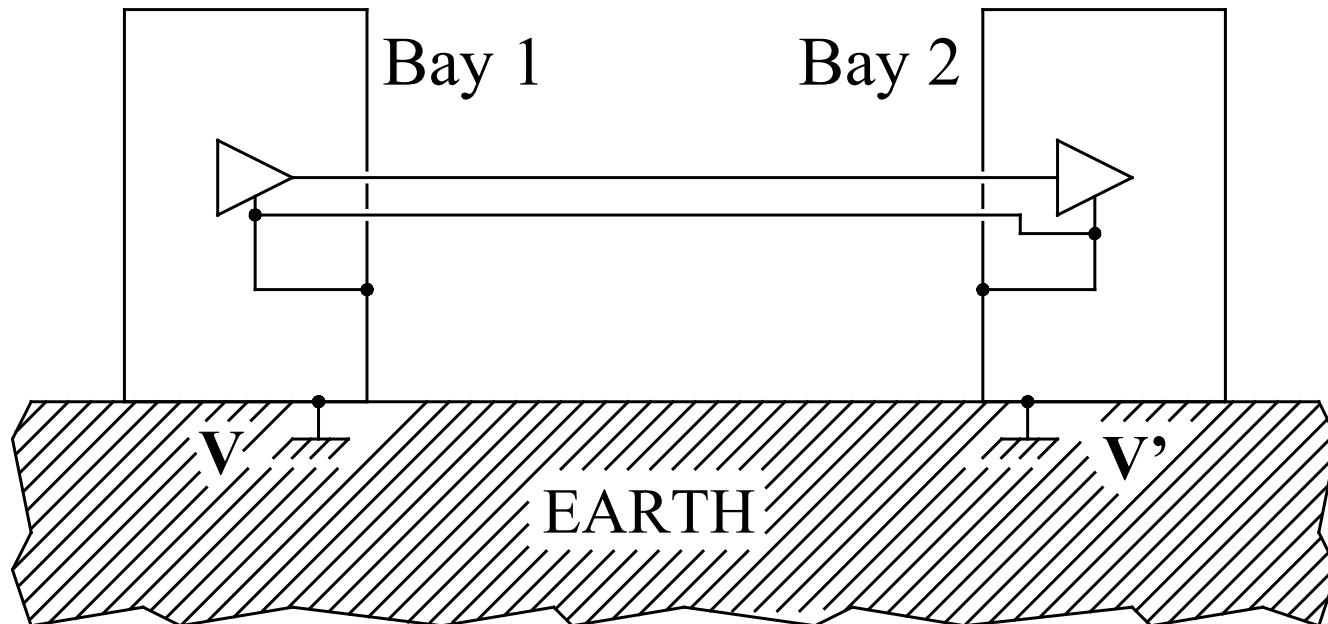
L2- Ground.



Where does signal's return current flow?

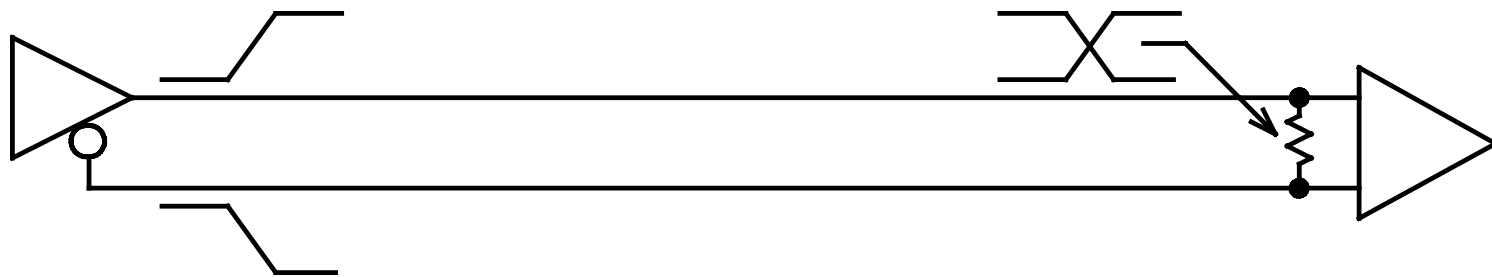
- Differential Pairs -

- First used to transmit signals between bays of super computers or bays / racks on the factory floor.
- Single ended lines (shown here) connecting large bays can have ground currents flowing even when signals are not present, creating offset errors.

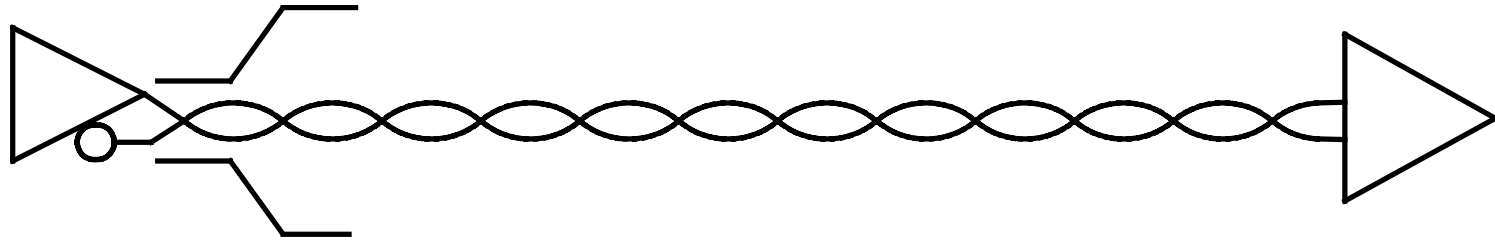


- Differential Pairs -

- In its basic form a Diff Pair consists of two transmission lines, containing equal amplitude but opposite polarity signals.
- The Receiver of the Differential Signals is a Crossing Detector -



- Differential Pairs -



- When transmitted in a Twisted Wire Pair -
 - Have tight containment of E and H Fields.
 - Lines use each other as a path for return current.
 - Have tightly controlled impedance.
 - Input ignores Unit-to-Unit ‘Ground’ Offsets.
 - Input has Common Mode Rejection of RF Noise.
- How does this apply to PC Boards?

- Differential Pairs -

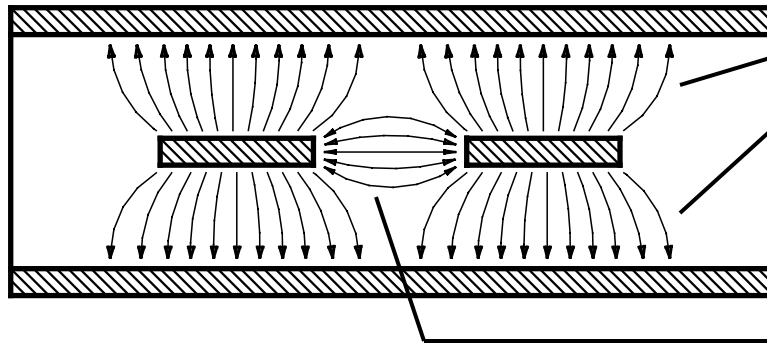
- Transmitted in a PC Board -
 - 2 Signals in 2 Transmission Lines.
 - Most of the Return Current for each line is in the Gnd / Pwr Planes of PC Board.
- Advantages vs Single Ended signals -
 - Input ignores Unit-to-Unit ‘Ground’ Offsets.
 - Will still function even with 10 to 15 dB of loss. Some logic families can tolerate 20 dB of loss.
 - Input has Common Mode Rejection of RF Noise (if and only if noise is induced equally into both lines).

- Differential Pairs -

- Differential Impedance -

- $Z_{\text{DIFF}} = 2 \times Z_{\text{ODD}}$

- $Z_{\text{ODD}} = Z_0 - Z_{\text{COUPLING}}$



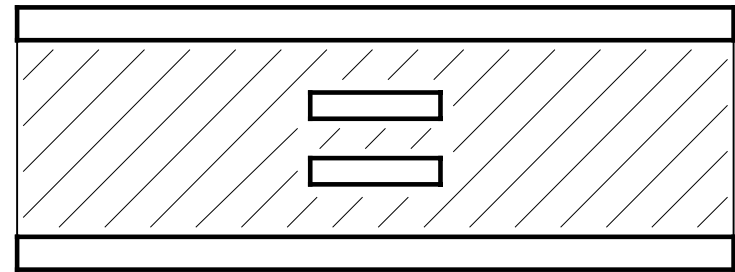
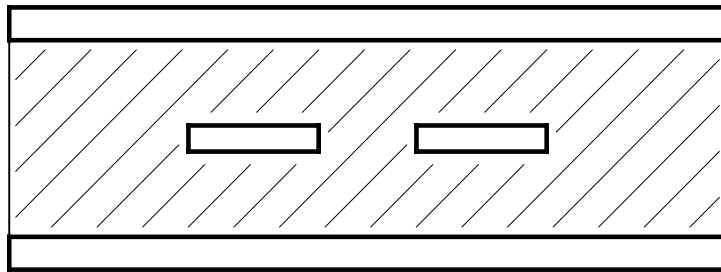
Fields That
Determine Z_0

Fields That
Determine Z_{COUPLING}

- Advantages and Disadvantages to High Z_{COUPLING}
- Use 2D Field Solver or Good Equation Based Tool

- Differential Pairs -

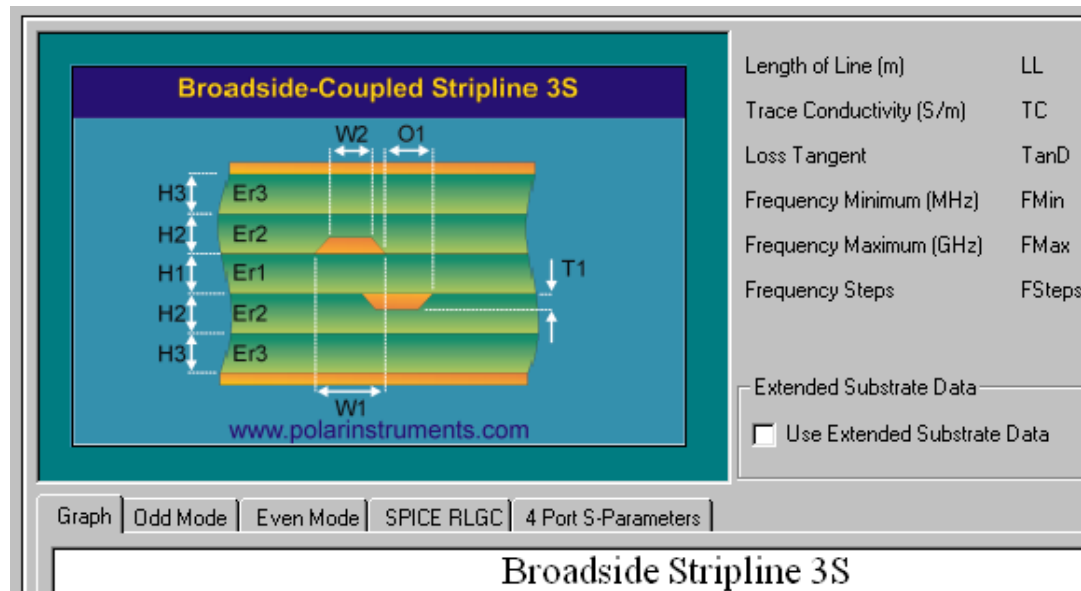
- Typically Routed Together, Side-by-Side (Edge Wise Coupled) or on Adjacent Layers (Broad-Side Coupled), at Approx the Same Length.
 - Intent is to get same RF Noise on each Line.
 - Minimized Skew (Within Limits of Skew Budget).



- Edge Coupled gives Greater Impedance Control, Either Characteristic or Odd Mode.
- Broad Side yields Higher Routing Density.

- Differential Pairs -

- To illustrate the concerns over impedance control in Broadside Coupled lines, Polar (in their Field Solvers), shows the potential offset.



- Typical shift of 5 mils can affect impedance by 10% or more (in addition to the normal +/-10%).

- Differential Pairs -

- Should Traces be Tightly Coupled?
- Reasons given for Tight Coupling -
 - Return current from one line travels in other line.
 - Reduces unwanted coupling from other signals.
- Tight Coupling does create different line widths in Pair than loose coupling.
 - Advantage: Narrower line per given impedance.
 - Disadvantage: Narrower line per given impedance.
- Narrower line is easier to route but can be hard to manufacture and harder to control impedance during manufacturing **AND**

- Differential Pairs -

- Z_{COUPLING} example (24" long routes)-



Source: Polar Field Solver

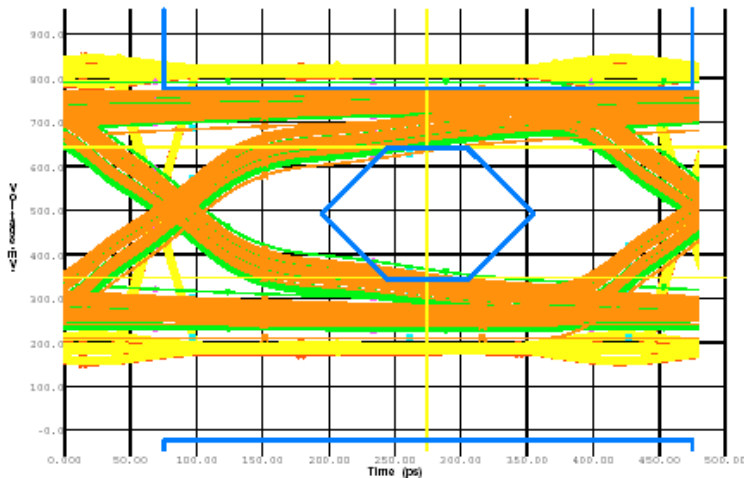
4 mil lines - 6.5 mil separation -

6 mils above plane - 100 Ω



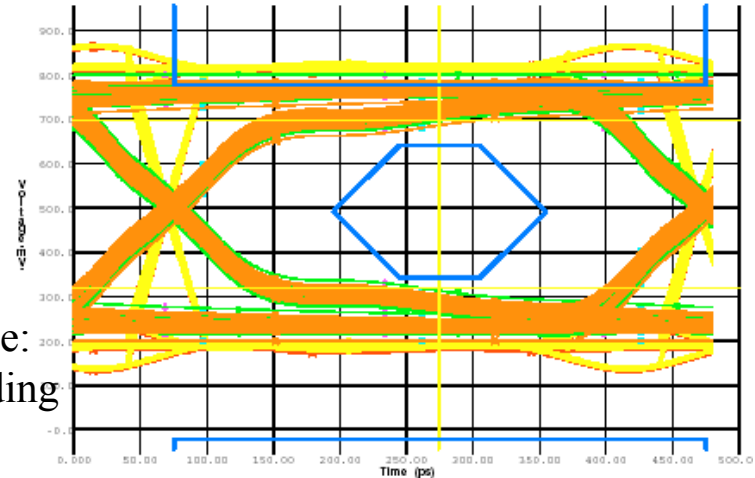
7 mil lines - 14 mil separation -

6 mils above plane - 100 Ω



4 mil lines - 3.125 Gb/S

Source:
Speeding
Edge



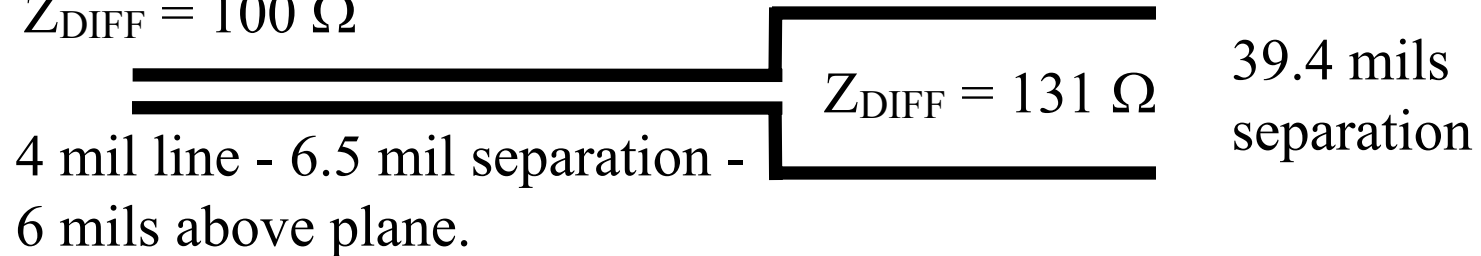
7 mil lines - 3.125 Gb/S

- Difference? --- Skin Effect!

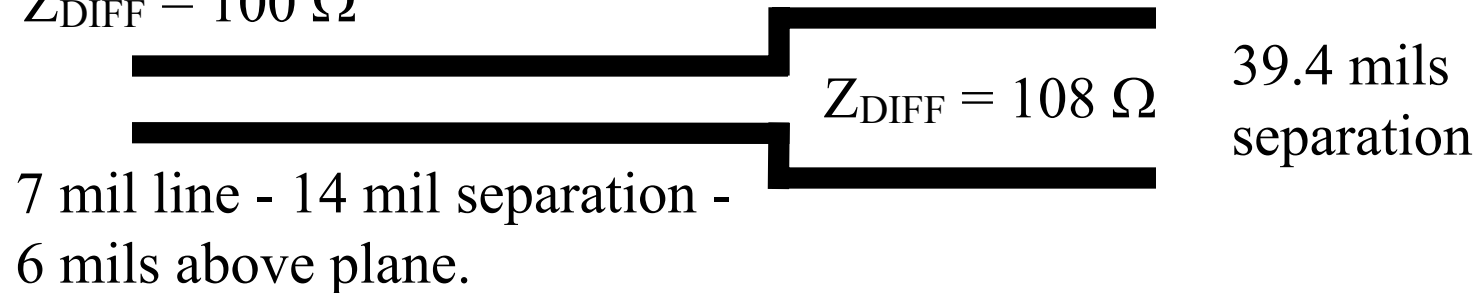
- Differential Pairs -

- Tightly Coupled lines Require constant spacing to maintain impedance close to 100 Ω .
- Separating lines to route through a 1 mm pitch BGA pin field will increase impedance.

$$Z_{\text{DIFF}} = 100 \Omega$$

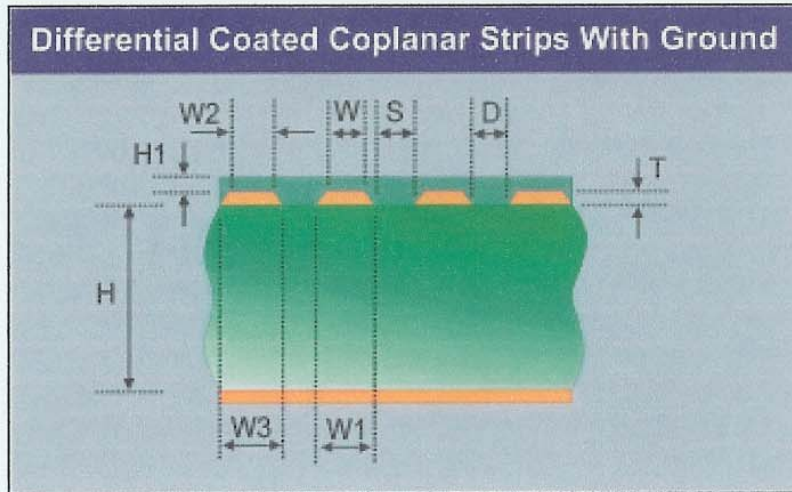


$$Z_{\text{DIFF}} = 100 \Omega$$



- Differential Pairs -

- 4 mil Lines - 6.5 mils Separation -

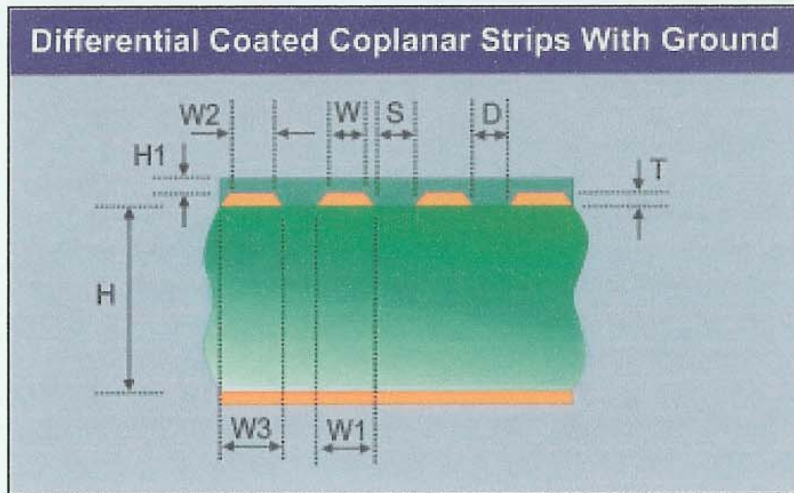


Height	H	6
Height1	H1	1
Width	W	4
Width1	W1	4
Width2	W2	250
Width3	W3	251
Thickness	T	2
Gnd Separation	D	50
Separation	S	<u>6.5</u>
Dielectric	Er	4.2

Diff. Impedance	Zo	<u>100.13</u>
Delay (ps/in)	D	156.291
Odd Mode	Zodd	50.06
Even Mode	Zeven	81.59
Common Mode	Zcomm	40.8

- Differential Pairs -

- 4 mil Lines - 39.4 mils Separation -

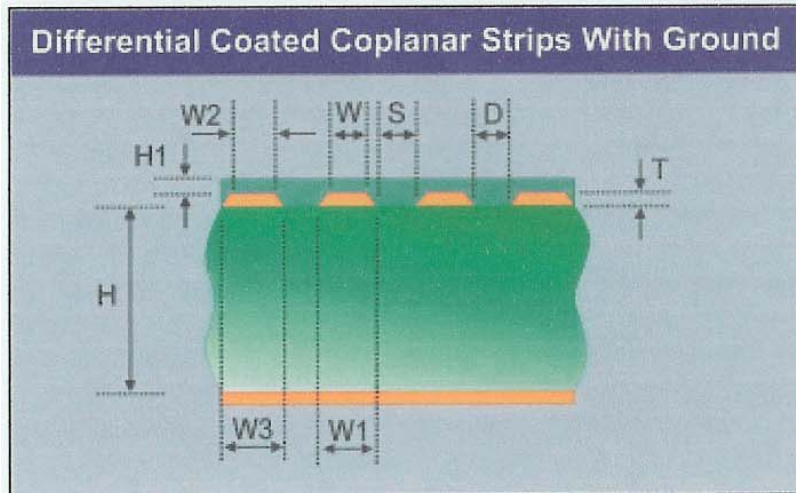


Height	H	6
Height1	H1	1
Width	W	4
Width1	W1	4
Width2	W2	250
Width3	W3	251
Thickness	T	2
Gnd Separation	D	50
Separation	S	<u>39.4</u>
Dielectric	Er	4.2

Diff. Impedance	Zo	<u>131.29</u>
Delay (ps/in)	D	157.104
Odd Mode	Zodd	65.65
Even Mode	Zeven	67.57
Common Mode	Zcomm	33.78

- Differential Pairs -

- 7 mil Lines - 14 mils Separation -

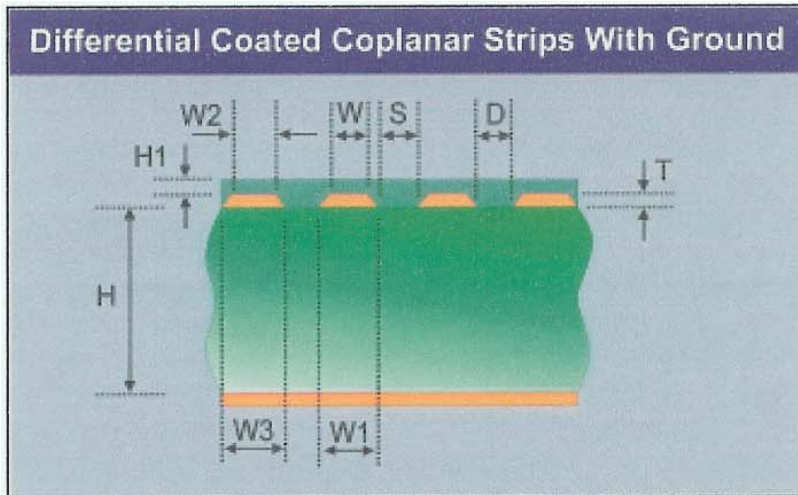


Height	H	6
Height1	H1	1
Width	W	7
Width1	W1	7
Width2	W2	250
Width3	W3	251
Thickness	T	2
Gnd Separation	D	50
Separation	S	<u>14</u>
Dielectric	Er	4.2

Diff. Impedance	Zo	<u>99.96</u>
Delay (ps/in)	D	154.939
Odd Mode	Zodd	49.98
Even Mode	Zeven	59.56
Common Mode	Zcomm	29.78

- Differential Pairs -

- 7 mil Lines - 39.4 mils Separation -



Height	H	6
Height1	H1	1
Width	W	7
Width1	W1	7
Width2	W2	250
Width3	W3	251
Thickness	T	2
Gnd Separation	D	50
Separation	S	<u>39.4</u>
Dielectric	Er	4.2

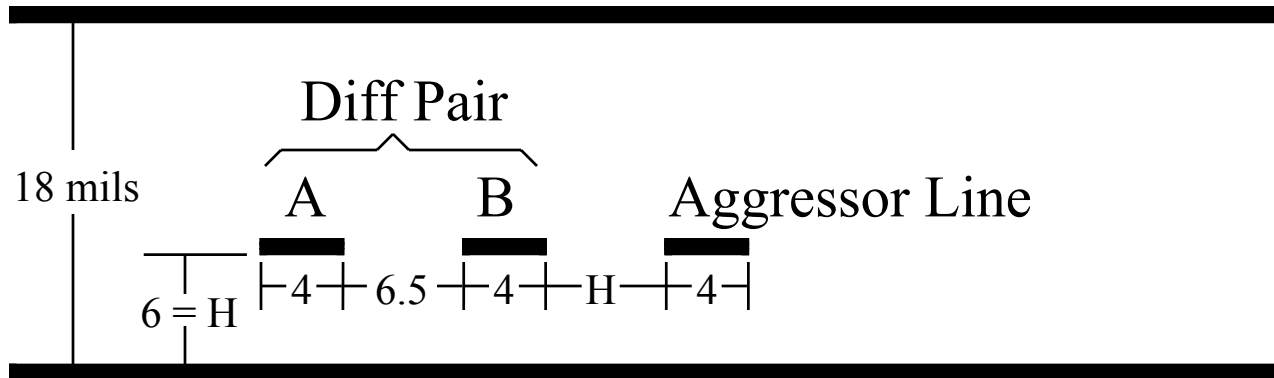
Diff. Impedance	Zo	<u>108.12</u>
Delay (ps/in)	D	157.163
Odd Mode	Zodd	54.06
Even Mode	Zeven	55.72
Common Mode	Zcomm	27.86

- Differential Pairs -

- Tightly Coupled traces in the Differential Pair work fine if -
 - Skin effect loss is not an issue (Routes are fairly short, ie- Under 10 to 12 inches - or frequency of circuit is under 1 GHz)
 - Lines do Not have to be separated during routing, to weave through a pin field (this could be a problem for BGAs with 1 mm or less pin pitch.
 - The Narrower lines are not TOO narrow and can be fabricated, and impedance controlled without difficulty.

- Differential Pairs -

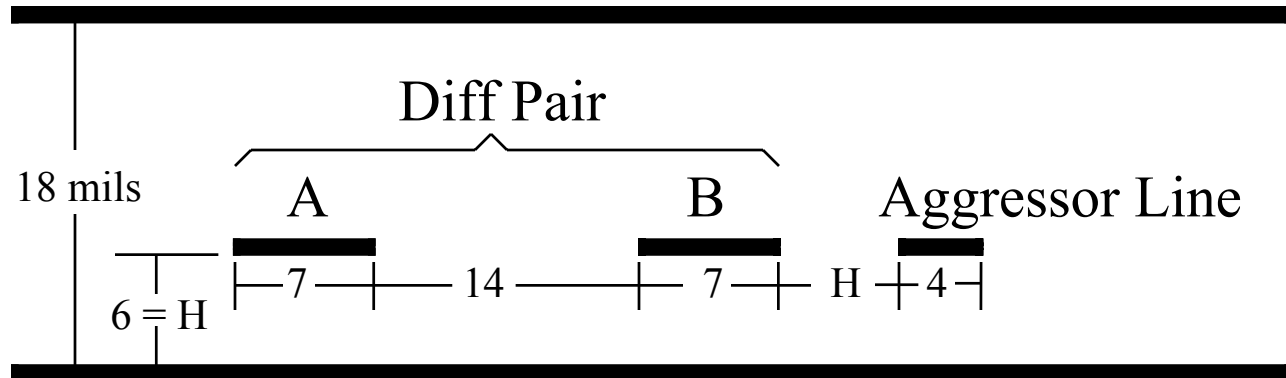
- Routing between planes -
 - Eliminates Coupling from External EM Fields.
 - Lowers Cross Talk, However -----



- Cross Talk from Aggressor to Line 'B' is 12%.
Cross Talk, Aggressor to Line 'A' is 2%.
- Tight Coupling does NOT make Cross Talk even.
Common Mode Rejection will not happen!!!

- Differential Pairs -

- With loosely coupled diff pair, Cross Talk from Aggressor to Line 'B' is still 12%. Cross Talk from Aggressor to Line 'A' is 1%.



- Cross Talk in the loosely coupled pair is only very slightly worse than the tightly coupled lines.
- Secret to Cross Talk control- Keep Aggressor far away from the Differential Pair.

- Differential Pairs -

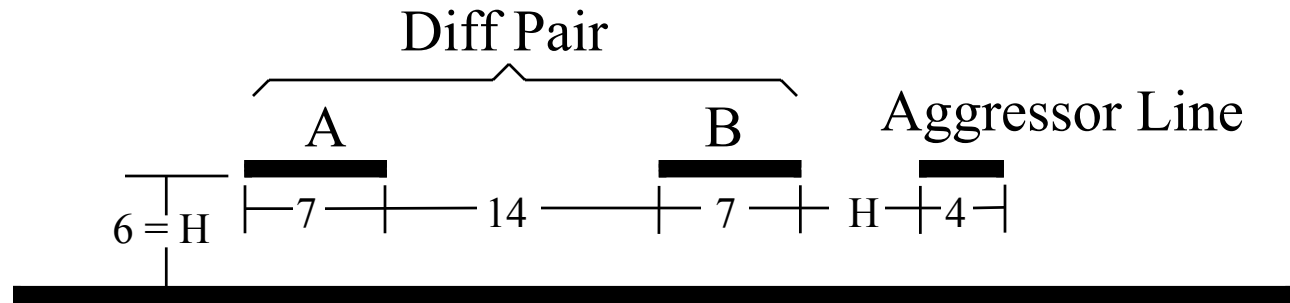
- Following table lists Cross Talk in the lines at various increments of 'H' (height above plane) -

<u>Trace 'B'</u> <u>to Aggressor</u>	<u>Coupling - 'A' and</u> <u>'B' - Tight Lines.</u>	<u>Coupling - 'A' and</u> <u>'B' - Loose Lines.</u>
2H	'B'= 3.5% - 'A'= 1.1%	'B'= 3.5% - 'A'= 0.3%
3H	'B'= 2.0% - 'A'= 0.5%	'B'= 2.0% - 'A'= 0.16%
4H	'B'= 0.8% - 'A'= 0.3%	'B'= 0.8% - 'A'= 0.12%
5H	'B'= 0.3% - 'A'= 0.15%	'B'= 0.3% - 'A'= 0.08%
6H	'B'= 0.1% - 'A'= 0.08%	'B'= 0.1% - 'A'= 0.04%

- Around 5H the coupling Difference is Low Enough that jitter from cross coupling will be minimized. At 6H difference is virtually gone.

- Differential Pairs -

- With Microstrip, the loosely coupled diff pair, Cross Talk from Aggressor to Line 'B' is 16%. Cross Talk to Line 'A' is 2.5%.



- Line A to Line B Cross Talk Difference in Microstrip is much more severe than Stripline.
- Keeping Aggressor far away is even more critical in outer layer transmission lines.

- Differential Pairs -

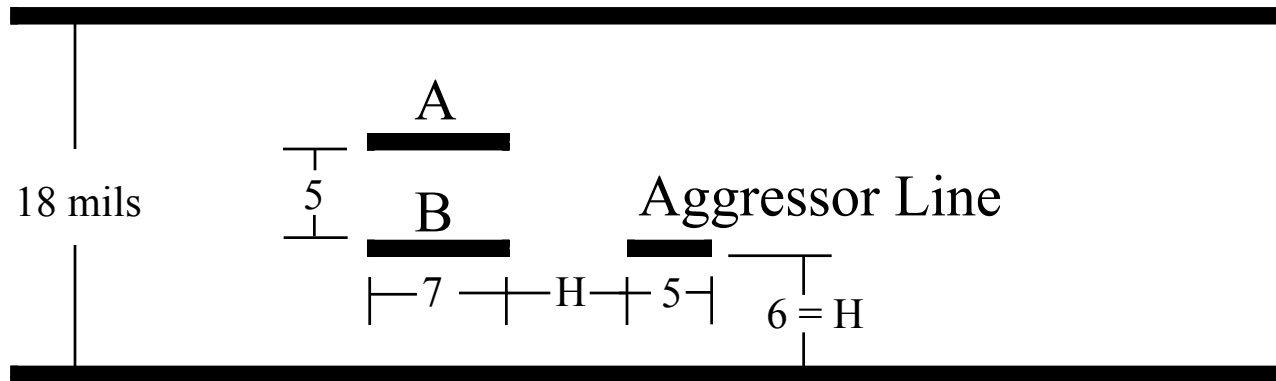
- Following table lists Cross Talk in the Microstrip lines at various increments of 'H' -

<u>Trace 'B'</u> <u>to Aggressor</u>	<u>Coupling - 'A' and</u> <u>'B' - Tight Line.</u>	<u>Coupling - 'A' and</u> <u>'B' - Loose Line.</u>
1H	'B'= 16.0%- 'A'= 4.3%	'B'= 16.0%- 'A'= 2.5%
2H	'B'= 7.0% - 'A'= 2.7%	'B'= 7.0% - 'A'= 1.7%
3H	'B'= 3.6% - 'A'= 1.8%	'B'= 3.6% - 'A'= 1.4%
4H	'B'= 2.7% - 'A'= 1.5%	'B'= 2.7% - 'A'= 1.1%
5H	'B'= 1.8% - 'A'= 1.1%	'B'= 1.8% - 'A'= 1.0%
6H	'B'= 1.3% - 'A'= 1.0%	'B'= 1.3% - 'A'= 0.9%

- Since Microstrip Cross Talk is greater, coupling Difference is about the same at 6H as Stripline Coupling at around 4H..

- Differential Pairs -

- Cross Talk in Broadside Coupled Lines -



- In the Differential Pair above, coupling into 'B' is 12% and coupling into 'A' is 8%.

- 2H	B = 4.5%	A = 3.0%
- 3H	B = 2.0%	A = 1.4%
- 4H	B = 0.8%	A = 0.6%

- Differential Pairs -

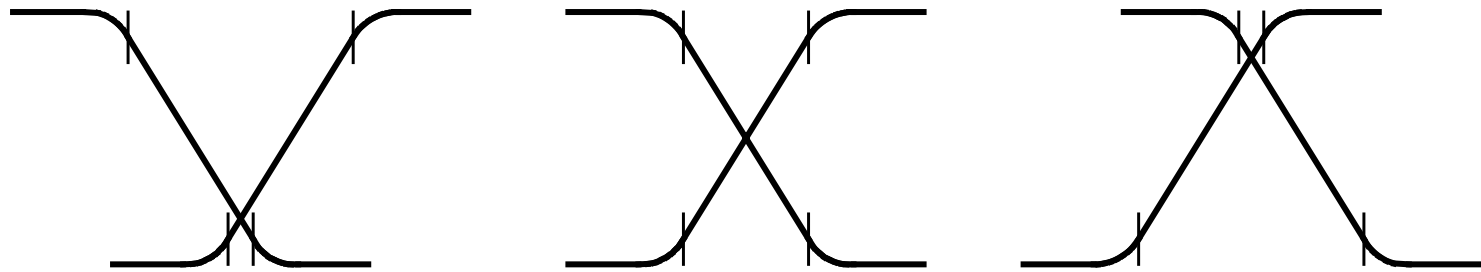
- Length Matching (Timing) Requirements -
 - Lengths of the 2 lines to be the Same within Limits set by Circuit Timing requirements.
- Don't follow an App Note, which states to route the two lines within 5 mils (or less) of one another!
- Look at circuit Timing!!!

- Differential Pairs -

- Length Matching -
- Simple solution -
 - Require that the two paths be length matched “as close as possible”.
 - This usually results in extreme difficulty routing the PCB. Take Designability into account to arrive at a circuit that is both routable and fully functional.
- Best solution -
 - Know how much timing skew is available within the IC logic families used and at the circuit frequency.
 - Match lengths close enough to Satisfy Skew Budget!

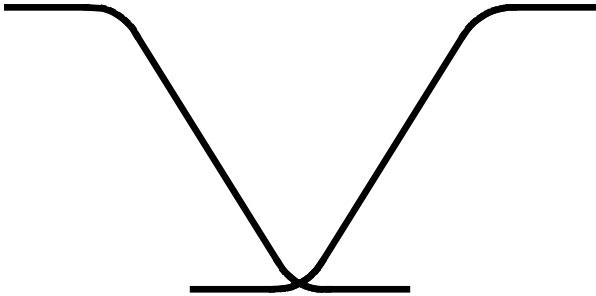
- Differential Pairs -

- Length Matching (Timing) Requirements -
 - Primary consideration, to keep Jitter to a minimum.
 - Jitter - Movement in time of the data crossing point from bit to bit with respect to the data path clock.
 - Jitter is Lowest when 2 signals cross straight portion of the rising and falling edges.



- All 3 sets of Waveforms will produce the Same Timing Jitter approximately Zero(0)!!!

- Differential Pairs -

- Signals below will still be detected as a proper crossing event - **But**, Edges that skew beyond limits of Linear Signal Edge WILL produce high Jitter!!!

- Crossing event moves around in time, relative to clock, due to uncertainty associated with Low Slope portion of waveforms.
- Jitter from this will be excessive and will likely render the circuit unusable.
- Stay within Skew Limits of rising signal edges.

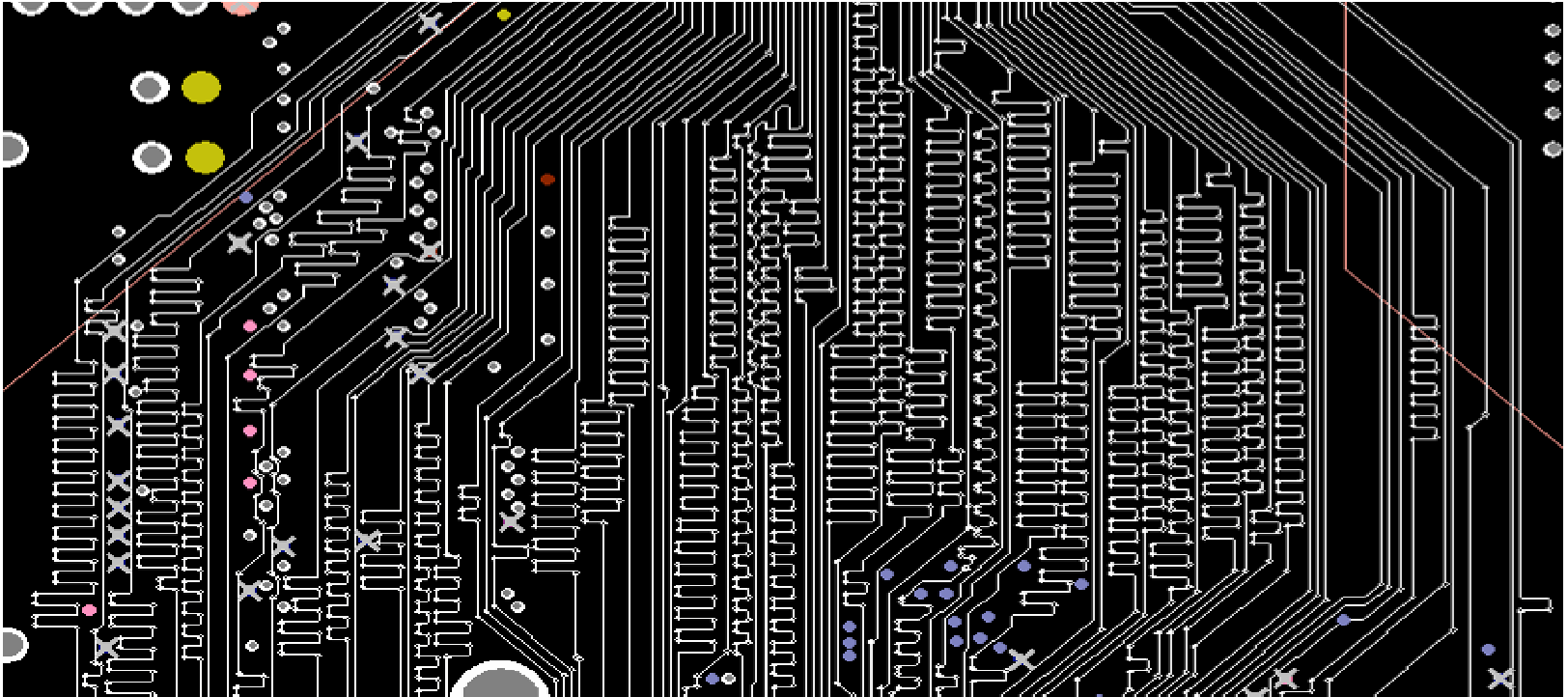
- Differential Pairs -

- Skew limits are set by the Fastest rise and fall times of the signals at the Receiver.
- Multiply fastest edge time by prop velocity in PC board [6 mils(.15mm) / Ps in most dielectrics].
- Result yields the Skew Budget -

<u>Circuit Speed</u>	<u>Available Skew</u>	<u>Length in mils (mm)</u>
256MHz	390 pS	2340 mils (59.4 mm)
266MHz	375 pS	2250 mils (57.2 mm)
1.2 Gb/S	160 pS	960 mils (24.4 mm)
2.4 Gb/S	80 pS	480 mils (12.2 mm)
3.125 Gb/S	62 pS	372 mils (9.45 mm)
10.0 Gb/S	20 pS	120 mils (3.05 mm)

- Differential Pairs -

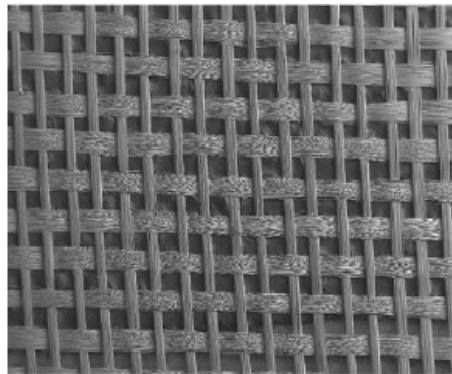
- What happens when designers get overly zealous about length matching of transmission lines!!!



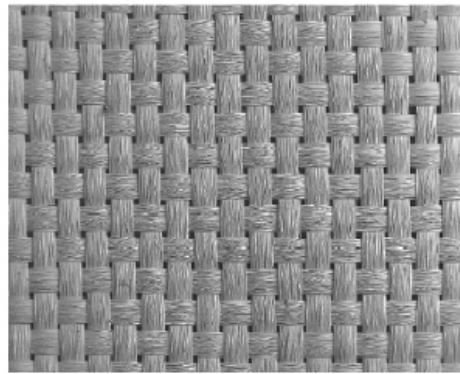
This was a wide, single ended bus, operating at approx 500 MHz, with margin of +/- 0.75 inch, yet lines were held to +/- 5 mils length.

- Differential Pairs -

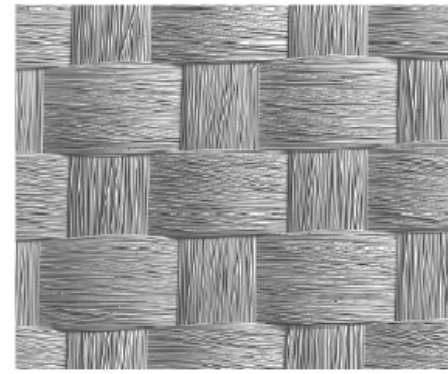
- How does PCB Material impact Skew Mismatch?
 - With some styles of Fiberglass weave, the yarn pitch can cause the 2 signal lines of the differential pair to sit on areas of vastly different Er.



1080



2116



7628

- With 3, 4 & 5 mil lines, closely spaced, on a layer with 1080 or 106 style glass, one of the diff pair lines may sit on an epoxy area and one on a fiber yarn.

- Differential Pairs -

- Skew Mismatch in Materials (Continued) -
 - The two lines may see ϵ_r difference as large as 0.5
 - Since signal Prop Delay = $\sqrt{\epsilon_r} / c$ (11.78 inch/ns), an ϵ_r difference of 0.5 can cause skew of 10 ps / inch.
 - With Gbit switching rates, lines longer than a few inches will see more skew than their budget allows.
- Per previous slide, problem only occurs with loosely woven fiberglass (ie - 106 or 1080).
- With tight weave, ϵ_r differences average out over very short distances.

- Differential Pairs -

Solution to Skew Mismatch in Materials -

- 1) Do Not spec materials with loosely woven fabric, such as 106 or 1080 (This is nearly impossible when designing high layer count or thin boards).
- 2) Have PCB fabricated with glass on a 45° bias, relative to the diff pair lines. (Extremely expensive, as the panel (18 x 24, etc,) will yield many fewer boards.)
- 3) Do Not route differential pairs in long, straight lines. Change direction often (can be Very difficult).
- 4) Spec flat, tightly woven glass, such as the types from *Dielectric Solutions, LLC* (Also low loss & low DK).

- Differential Pairs -

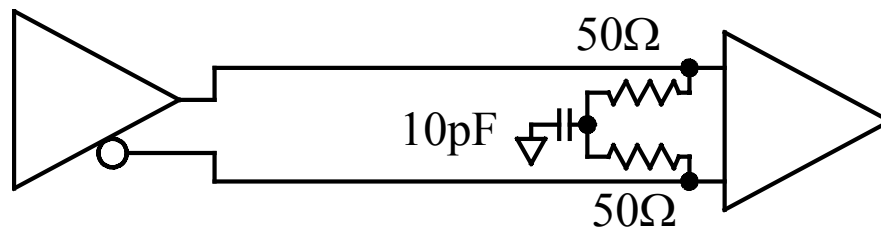
- Concerns with minor timing mismatch -
- There are a couple caveats to the skew issues discussed -
 - If Differential Pair routes through a ‘Non-Grounded’ connector, signals must be aligned within a few pSec or fields DO NOT couple tightly and noise or EMI will likely result.
 - This is true whether routing board-to-board or into a cable or twisted pair!
- The second concern with misalignment of signals has to do with possible ‘Bit Error Rate’ issues.

- Differential Pairs -

- When signals do Not cross at midpoint, there is short time interval when current must flow into or out of Vref terminal.
- If Termination is a single 100 ohm resistor there is no connection from the lines to Vref.
- With No path to Vref, current is not available and one signal edge slows down.
- At low data rates (LVDS or 266MHz, etc), edge degradation from slowing is not an issue.
- If data rates are high (short bit intervals) this issue can affect 'Bit Error Rate'.

- Differential Pairs -

- Certainly an issue at 2.4 Gb/S and higher rates.
- Solutions -
 - Thevenin termination on each end of line (increases power consumption and uses excess real estate).
 - Best solution, two 50Ω termination resistors, with common pins connected through small capacitor to V_{ref} .

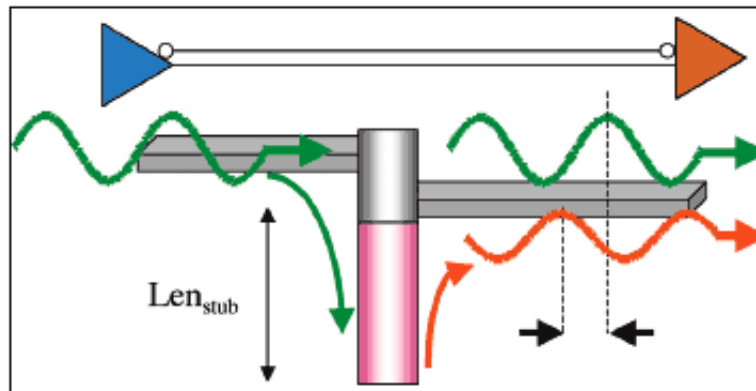


- At gigabit rates and higher, may be necessary to locate Terminations on die (to preserve signal integrity). Look for these type ICs.

- Vias in Differential Pairs -

- Via Discontinuity -

- A via Stub (shown in pink) is a Capacitive Discontinuity when length is close to $1/4 \lambda$ (in DK) of a signal. When distance for energy to travel



into the stub (green arrow), Reflect and travel back (Red arrow) is $1/2 \lambda$, 180° reflections on

- the line affect signal Jitter and Bit Error Rates.
- This happens in a 0.100" Stub at 30 Gb/Sec.

(Image Source: Dr. Eric Bogatin)

- Vias in Differential Pairs -

- Only discontinuities that are Electrically Long will cause ringing in circuits -
 - Vias in line are NOT a discontinuity in MOST circuits!
 - If length of via section is shorter than $1/20 \lambda$, via is ZERO discontinuity (0.100" via section has no effect up to 60 Gb/s).
 - Vias longer than $1/20 \lambda$ are extremely small discontinuity, if non-functional pads are removed.
 - Via stubs are only a discontinuity in very thick boards AND at GHz frequencies.
 - A 0.100" stub is a problem above 15 GHz (30 Gb/s).
 - Back-drilling Eliminates Stub!!!
 - Removing Non-Functional pads lower capacitance 30 - 40%.